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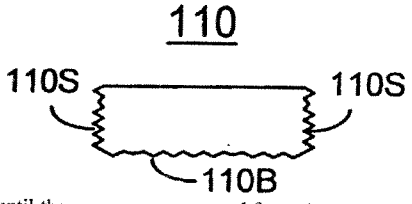
(54) Title: THINNING AND DICING OF SEMICONDUCTOR WAFERS USING DRY ETCH, AND OBTAINING SEMICONDUCTOR CHIPS WITH ROUNDED BOTTOM EDGES AND CORNERS



(57) Abstract: A semiconductor wafer is diced before thinning. The wafer is diced only part of the way through, to form grooves which are at least as deep as the final thickness of each chip to be obtained from the wafer. Then, the wafer is placed into a non-contact wafer holder, and the wafer backside is blanket etched with a dry etch, for example, atmospheric pressure plasma etch. The wafer is thinned until the grooves are exposed from the backside. The dry etch leaves the chip's backside smooth. After the grooves have been exposed, the dry etch is continued to remove damage from the chip sidewalls and to round the chips' bottom edges and corners. As a result, the chip becomes more reliable, and in particular more resistant to thermal and other stresses.

THINNING AND DICING OF SEMICONDUCTOR WAFERS USING DRY ETCH, AND OBTAINING SEMICONDUCTOR CHIPS WITH ROUNDED BOTTOM EDGES AND CORNERS

BACKGROUND OF THE INVENTION

The present invention relates to thinning and dicing of semiconductor wafers using a dry etch.

In many semiconductor fabrication processes, when circuitry has been fabricated in a semiconductor wafer, the wafer is thinned and then diced into chips. The thinning is typically performed with mechanical lapping. Dicing is performed with a diamond saw or a laser. The diamond saw or the laser can be used to cut the wafer all the way through along scribe lines. Alternatively, the wafer is cut part of the way through, and then broken.

The thinning and dicing processes can damage the wafer. It is desirable to provide alternative processes that reduce wafer damage and prolong the lifetime of chips obtained from the wafer.

SUMMARY

Some embodiments of the present invention reduce or eliminate wafer damage and prolong the chip lifetime by dicing the wafer part of the way through and then thinning the wafer with a dry etch. The chip lifetime is prolonged because the dry etch removes damage from chip surfaces and rounds the chip's edges and corners.

More particularly, as illustrated in Fig. 1, a chip 110 obtained by prior art thinning and dicing techniques may have uneven, damaged surfaces 110B, 110S, with sharp bottom corners and edges. Surface 110B is the chip's backside, and surfaces 110S are sidewalls. The wafer has been thinned from backside 110B by mechanical lapping, and then diced along sidewalls 110S with a diamond saw or a laser apparatus. These thinning and dicing processes damage the backside 110B and sidewalls 110S. The damage may include chipped, jagged surfaces, and microcracks. When the chip 110 is later packaged and put into use, the chip is subjected to heating and cooling cycles. These cycles cause the chip's

packaging material (not shown) to exert stresses on the chip. Additional stresses can be developed inside the chip due to the thermal cycles, chip handling, or the presence of different materials or other non-uniformities inside the chip. Because the chip surfaces 110B, 110S are damaged, and because they intersect at sharp edges and corners, the stresses concentrate at isolated points on the chip surface. Further, microcracks weaken the chip's resistance to stress. As a result, the chip becomes less reliable. Cracks formed or extended by stresses in the chip can reach and damage the chip circuitry (not shown).

Dry etch provides smoother chip surfaces and rounded edges and corners. Damage is reduced or eliminated. The chip reliability is therefore improved.

In some embodiments of the present invention, the wafer is processed as follows. The wafer is diced to form grooves in the face side of the wafer. The grooves are at least as deep as the final thickness of each chip to be obtained from the wafer. Dicing can be performed with a diamond saw or a laser. The grooves' sidewalls can be damaged.

Then the wafer is placed into a non-contact wafer holder, and the wafer backside is etched with the dry etch until the grooves are exposed from the backside. The dry etch leaves the chips' backside smooth. In some embodiments, the dry etch continues after the grooves have been exposed from the backside. The etchant gets into the grooves and smoothens the chip sidewalls, removing at least some of the sidewall damage. The etchant also rounds the bottom corners and edges of the chips.

Suitable etches include atmospheric pressure plasma etches described, for example, in the PCT Application PCT/US97/18979 (WO 98/19337) filed October 27, 1997, incorporated herein by reference. These etches are fairly fast. Silicon can be etched at 10 μm/min.

In some embodiments, the dry etch is a blanket uniform etch of the wafer's flat backside surface. No masking layers are used on the backside surface.

The invention is not limited to the embodiments described above. In some embodiments, one or more openings are formed in a first surface of a semiconductor wafer along a boundary of one or more chips. The openings do not go through the wafer. The

wafer is placed into a non-contact wafer holder and thinned with a dry etch until the openings are exposed on a second side.

Other features of the invention are described below. The invention is defined by the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a side view of a prior art semiconductor chip.

Fig. 2A is a top view of a wafer being processed according to an embodiment of the present invention.

Fig. 2B shows a cross-section of the wafer of Fig. 2A along the lines II - II.

Figs. 3 and 4 are cross-sections illustration of a wafer and processing equipment during wafer thinning according to an embodiment of the present invention.

Fig. 5 is a perspective view of a chip processed according to an embodiment of the present invention.

Fig. 6 is a side view of a packaged chip processed according to an embodiment of the present invention.

Figs. 7 through 11 are cross-section illustrations of wafers being processed according to embodiments of the present invention.

DESCRIPTION OF SOME EMBODIMENTS

Fig. 2A is a top view of a semiconductor wafer 210 shown before the wafer is thinned with a dry etch. Fig. 2B is a cross sectional view of the wafer along the lines II-II in Fig. 2A. Circuitry has been fabricated in the wafer, and the wafer must now be divided into chips 110. The circuitry may include transistors, diodes, and other devices (not shown) manufactured in and over an active layer 220 (Fig. 2B) adjacent to the wafer top surface 210F (the surface shown in Fig. 2A). Optional conductive bumps 216 have been

manufactured on contact pads on top surface 210F of chips 110. The bumps will be used to connect the chips to wiring substrates (not shown), e.g., printed circuit boards.

The wafer thickness 240 has been sufficiently large to achieve suitable mechanical strength and heat dissipation during fabrication of the wafer circuitry. 720 μm is suitable for some silicon wafer fabrication processes. The wafer will now to be thinned to its final thickness 250. In some embodiments, the final thickness is 10-450 μm. These thickness figures are illustrative and not limiting.

After the circuitry and the bumps 216 were manufactured, grooves 260 were formed in the wafer top surface along scribe lines and, in particular, along the boundary of chips 110. The grooves could be formed by conventional dicing techniques, e.g. with a diamond saw or a laser. Other processes, e.g., a masked etch, could also be used. The grooves do not go through the wafer. The grooves are at least as deep as the final chip thickness 250. In some embodiments, the groove depth is 10-450 μm. The grooves will be exposed from the bottom during wafer thinning when the wafer back side 110B is etched, as described below.

The groove sidewall and bottom surfaces 270 can be damaged by dicing, as schematically shown by uneven lines in Figs. 2A, 2B.

Wafer 210 is placed in a non-contact wafer holder 510 (Fig. 3). Holder 510 includes one or more vortex chucks 520 having outlets in the holder's surface 524. Surface 524 faces the top surface of the wafer. Gas supplied under pressure through a conduit 522 enter chucks 520 through respective passages 523. Each passage is tangential to the chuck's cylindrical chamber when viewed from the top. A gas vortex 525 emitted by each chuck towards the wafer generates a low pressure zone near the chuck's vertical axis. In this zone, the wafer is drawn towards the chuck. At the same time, the gas vortices do not allow the wafer to touch the holder surface 524. Such wafer holders are described, for example, in U.S. patent application no. 09/456,135 "Non-Contact Workpiece Holder" filed by O. Siniaguine et al. on December 7, 1999 and incorporated herein by reference. Other suitable holders are described in PCT publication WO 99/46805 (TruSi Technologies, LLC, September 16, 1999) incorporated herein by reference. Other holders, for example, Bernoulli type holders, can also be used.

Wafer holder 510 is called "non-contact" because the top surface of the wafer does not contact the holder surface 524. However, the edge of the wafer can contact the holder's limitors 526 which extend around the wafer to restrict the wafer lateral motion. In some embodiments, holder 510 is mounted on a rotating carousel (not shown). The carousel rotation develops a centrifugal force that presses the wafer against one or more limitors 526. See PCT publication WO 99/26796 (TruSi Technologies, LLC, June 3, 1999).

The wafer backside surface 110B is etched with a dry etch. In Fig. 3, the etch is a blanket (unmasked) uniform etch of the wafer's flat semiconductor backside surface (e.g., silicon surface). The etch is atmospheric pressure plasma etch. Plasma generator 530 generates plasma 540 into which suitable reagents are injected. If the wafer is made of silicon, a CF4 etch can be used. See PCT publication WO 98/19337 (TruSi Technologies, LLC, May 7, 1998) incorporated herein by reference. A suitable etcher is type Tru-Etch 3000 (trademark) available from TruSi Technologies, LLC, of Sunnyvale, California. The dry etch thins the wafer until the grooves 260 are exposed from the bottom. When the grooves are exposed, the plasma enters the grooves and etches the groove sidewalls 270. The sidewalls become smoother as a result. The dicing damage becomes partially or completely removed from the sidewalls. The bottom corners and edges of chips 110 become rounded.

Advantageously, some atmospheric pressure plasma etching processes described in WO 98/19337 are fast. Silicon can be etched at the rate of about 10 μm/min. Other kinds of etches can also be used. The dry etch can be preceded by mechanical lapping of the wafer bottom surface 110B.

In some embodiments, before the backside etch, the groove depth 250 (Fig. 2) exceeds the final chip thickness by an amount needed to obtain the rounded edges and corners and smooth sidewalls for chips 110. The more the groove depth exceeds the final chip thickness, the longer the duration of the backside etch after the grooves have been exposed from the bottom. The bottom corners and edges become more rounded, and more time is allowed for sidewall damage removal. In some embodiments, the radius of the rounded corners is roughly 1.5 times the thickness of the material removed from the wafer backside after the grooves are exposed. The depth of the grooves also takes into account possible wafer non-uniformity, the non-uniformity of the dicing process that creates the

grooves, and the non-uniformity of the backside etch. If mechanical lapping or any other process is used to remove material from the wafer backside before the dry etch illustrated in Fig. 5, the non-uniformity of such process can also be taken into account. In some embodiments, the groove depth 250 exceeds the final chip thickness by 10 μm or more.

When the grooves 260 become exposed during the thinning etch of Fig. 3, chips 110 become separated from each other, but the chips are held in holder 510 by the vacuum forces developed by the gas vortices. The vortex chucks 520 are positioned close to each other to insure that each chip 110 will be adjacent to a low pressure zone developed by at least one chuck 520. In Fig. 4, "L" denotes the greatest lateral dimension of each chip 110. "P" is the distance between the centers of the adjacent chucks 520. "D" is the diameter of each chuck. "P" and "D" can vary for different chucks 520 in the same wafer holder. The diameter D of each vortex chuck should be small enough to prevent a chip from being sucked into the chuck. The chip should be balanced at a predetermined distance from the wafer holder surface 524 by the vacuum forces drawing the chip towards the holder and the opposite-direction forces generated between the chucks by the gas flowing away from the chucks. In some embodiments, $D < L/2$ and $P < L/2$ for all the chucks.

In some embodiments, each of P and D is less than one half of the shortest side of each rectangular chip 110.

In some embodiments, the distance between the adjacent chucks and the diameter of each chuck take into account the peripheral wafer portions 320 (Fig. 2A). Each of P and D is less than one half of the greatest lateral dimension, or of the longest or shortest side, of each portion 320.

Fig. 5 is a perspective view of a chip 110 after the etch. The chip is shown bottom side up. The chip's sidewalls 110S and bottom surface 110B are smooth. The edges 110E at which the sidewalls 110S meet with each other and with the bottom surface 110B are rounded, and so are the bottom corners 110C. The smooth surfaces and the rounded edges and corners prolong the chip's lifetime and improve the chip's reliability.

In Fig. 6, chip 110 has been mounted on a printed circuit board 610 using flip chip technology. Bumps 216 are soldered to the printed circuit board. Encapsulant 620 (suitable plastic) is deposited over the chip for protective purposes. The chip's smooth

surfaces and rounded edges and corners prolong the chip's lifetime. Similar advantages are achieved with non-flip-chip packaging.

In Fig. 7, the etch uniformity is improved by depositing a layer 310 over grooves 260 and wafer portions adjacent to the grooves. Layer 310 is deposited before the backside etch of the wafer. When chips 110 and peripheral portions 320 become separated during the backside etch, the layer 310 holds the chips and the portions 320 in the same position relative to each other. Therefore, the gaps between the chips 110 and the peripheral portions 320 remain uniform, and hence the chip sidewalls (the sidewalls of grooves 260) are etched uniformly. If some chips 110 were too close to each other or to peripheral portions 320, the chips' sidewalls could be etched too slowly, and less damage would be removed than desirable. Other sidewalls, farther from adjacent chips 110 or portions 320, could be undesirably overetched.

Layer 310 also relaxes the requirements for the distance between adjacent vortex chucks 520 and the diameter of each chuck since the chips 110 and peripheral portions 320 are held in position by layer 310 throughout the backside etch.

Layer 310 can be a sticky material which adheres to the wafer without additional adhesive. Alternatively, adhesives can be used. In some embodiments, layer 310 is polyimide. Polyimide is chosen because it does not react with etchants utilized in some thinning processes (e.g., CF4). The thickness of polyimide layer 310 is 1 μm to 200 μm in some embodiments. Other materials and thicknesses can also be used. In some embodiments, layer 310 is an adhesive tape such as described in US patent 5,888,883 issued on March 30, 1999 to Sasaki et al.

Layer 310 does not cover the middle portions of chips 110, including the bumps 216. The bumps, and any other uneven features of the chip top surface 210F, are believed to be capable of impeding adhesion of layer 310 to the wafer.

In some embodiments, layer 310 is pre-manufactured as a continuous sheet. Then openings are cut out in layer 310 at the location of the middle portions of chips 110. Then layer 310 is deposited.

Layer 310 can be deposited using known techniques. In some embodiments, layer 310 is deposited at atmospheric pressure using a roller to remove air bubbles. Alternatively, layer 310 can be laminated on the wafer in vacuum, with or without a roller.

In some embodiments, layer 310 covers peripheral portions 320. In Fig. 8, layer 310 covers the entire wafer. In some embodiments, the top surface of chips 110 is even, bumps 216 are absent.

The invention is not limited to layer 310 covering or exposing any particular features of the wafer.

Layer 310 prevents the plasma from going through the grooves 260 and damaging the circuitry at the top surface of the wafer. Gas emitted by chucks 520 flows down around the wafer as shown at 550 in Fig. 3, and impedes the plasma from flowing up around the wafer and reaching the wafer top surface. As indicated in the aforementioned U.S. patent application 09/456,135, the chuck density can be made high at the edge of wafer holder 510 to prevent the plasma from flowing up around the wafer. Gas can be made to flow down at all points around the wafer.

In Fig. 9, layer 310 has been deposited by a spin-on or spraying technique. Layer 310 fills grooves 260. (In contrast, in Figs. 7 and 8, the grooves are not filled.) Layer 310 in Fig. 9 can be polymer or some other material.

Fig. 10 shows the structure after the backside etch for Fig. 9. In the embodiment of Fig. 10, when layer 310 is exposed from the bottom, layer 310 is etched faster than the wafer substrate. Therefore, the bottom surface of layer 310 is higher than the bottom surface of chips 110 and peripheral portions 320. The bottom corners and edges of chips 110 have been exposed to the etchant, and have been rounded.

Fig. 11 illustrates an embodiment in which the layer 310 is etched slower than the wafer substrate. This is the case if layer 310 is polyimide, the wafer is a silicon wafer, and the etch is a CF4 plasma etch. Layer 310 is etched slowly, but the microloading effect causes the chips 110 to be etched faster at the bottom edges adjacent to layer 310. As a result, the bottom edges and corners of chips 110 are rounded.

After the etch of Fig. 10 or 11, layer 310 is removed. In some embodiments, polyimide layer 310 is removed by oxygen plasma.

The above embodiments illustrate but do not limit the invention. The invention is not limited to silicon wafers or any packaging technology. The invention is not limited to plasma etching, or to any particular etch chemistry or type of etcher. The invention is not limited to wafers containing multiple chips. In some embodiments, only one chip has been

fabricated in the wafer. The chip is extracted and the wafer peripheral portions 320 are discarded. The invention is not limited to unmasked or uniform backside etches. Other embodiments and variations are within the scope of the invention, as defined by the appended claims.

CLAIMS

1. A method for obtaining one or more chips from a semiconductor wafer, the method comprising:

forming one or more openings in a first surface of the semiconductor wafer along a boundary of the one or more chips, wherein the one or more openings do not go through the wafer; and

placing the wafer into a non-contact wafer holder and thinning the wafer with a dry etch to remove material from a second side of the wafer at least until the openings become exposed on the second side.

2. The method of Claim 1 wherein the one or more openings comprise a groove extending along the entire boundary of at least one chip.

3. The method of Claim 2 wherein the wafer holder comprises one or more vortex chucks each of which emits a gas vortex towards the wafer to hold the wafer in the holder.

4. The method of Claim 2 further comprising, after forming the one or more openings but before thinning the wafer, attaching the first side of the wafer to a layer which remains on the wafer while the wafer is thinned.

5. The method of Claim 2 further comprising, after forming the one or more openings, forming a protective layer on the first side over the openings, the protective layer protecting the first side of the wafer during the dry etch from an etchant penetrating through the openings from the second side and damaging the first side when the openings become exposed on the second side.

6. The method of Claim 5 wherein the layer does not cover the entire first side of the wafer.

7. The method of Claim 5 wherein the layer covers the entire first side of the wafer.

8. The method of Claim 2 wherein the dry etch comprises an atmospheric pressure plasma etch.

9. The method of Claim 2 wherein after the groove is exposed from the second surface, the dry etch continues and smoothens the groove's sidewall.

10. The method of Claim 2 wherein the semiconductor wafer comprises circuitry made at the first side of the wafer, the second side is a backside opposite to the first side, and the groove is formed along a scribe line on the first side.

11. The method of Claim 2 wherein the groove is formed with a diamond saw or a laser.

12. The method of Claim 2 wherein the dry etch rounds one or more of the edges and corners which are obtained on the second side of the wafer when the one or more openings are exposed.

13. The method of Claim 12 wherein the dry etch rounds all of the edges and corners on the second side of each semiconductor chip obtained from the wafer in the dry etch.

14. The method of Claim 2 wherein from a start of the thinning operation until the groove is exposed, the dry etch etches the second side of the wafer uniformly.

15. The method of Claim 2 wherein the entire dry etch is an unmasked etch of the second surface.

16. A semiconductor chip obtained by the method of Claim 1.

17. A semiconductor chip obtained by the method of Claim 2.

18. A semiconductor chip obtained by the method of Claim 12.

19. A semiconductor chip obtained by the method of Claim 13.

20. A semiconductor ship having a first surface that has a rounded edge or a rounded corner.

21. The semiconductor chip of Claim 20 in which all of the edges and corners of the first surface are rounded.

22. The semiconductor chip of Claim 20 wherein the first surface is a back surface of the chip, the chip having circuitry formed at its front surface which is opposite to the back surface.

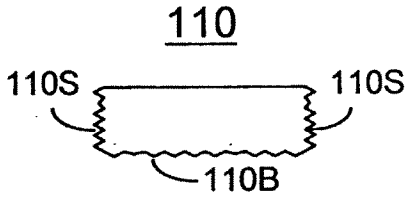
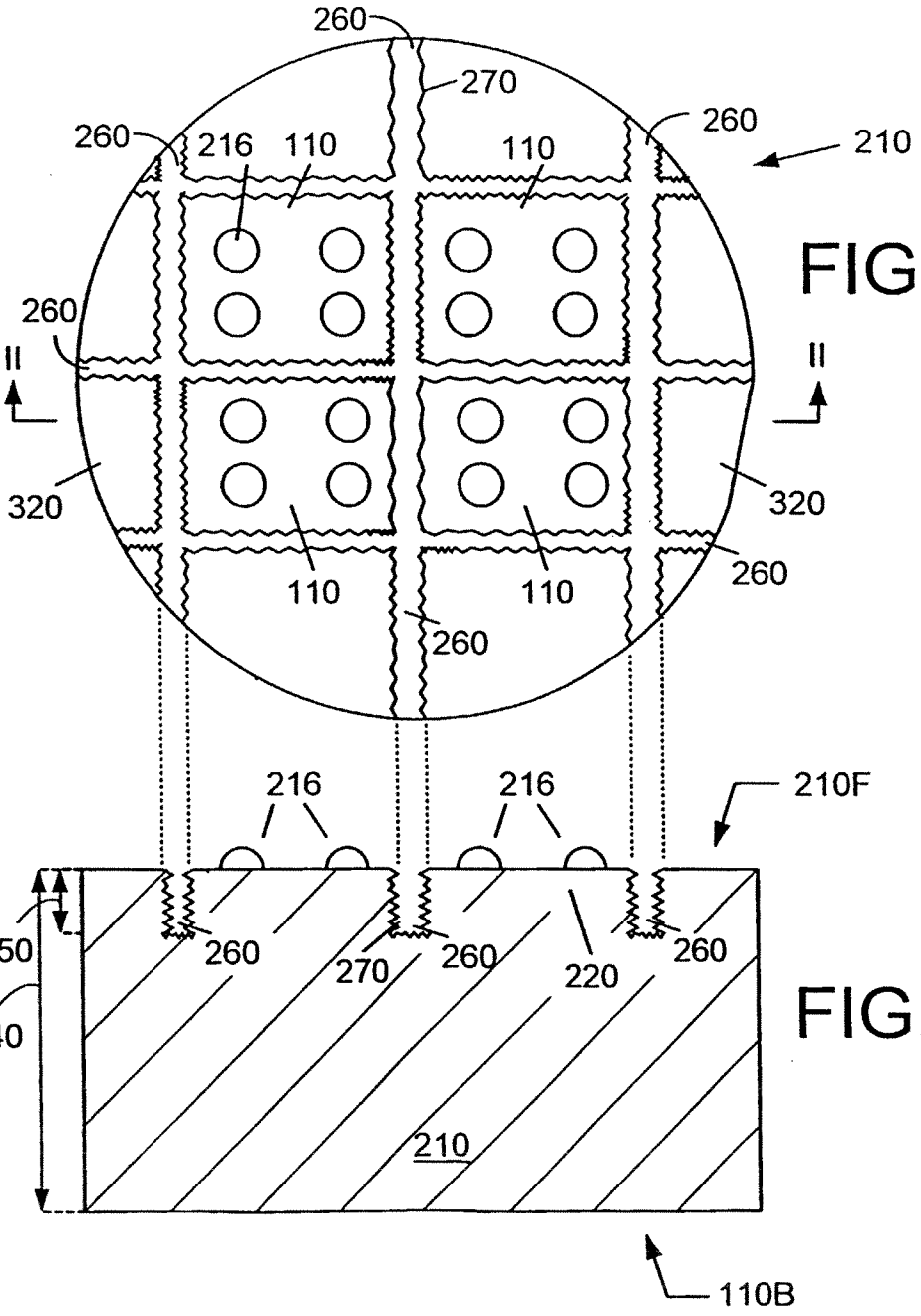


FIG. 1 PRIOR ART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220
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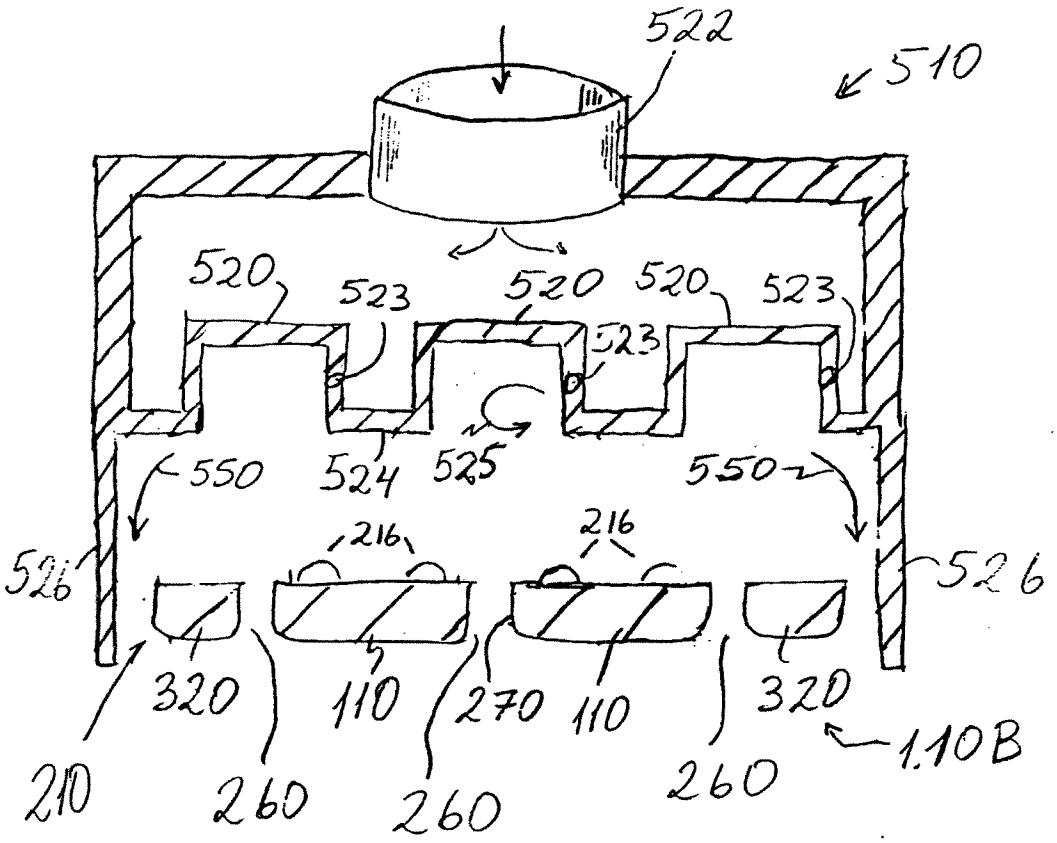
110B

FIG. 2A

FIG. 2B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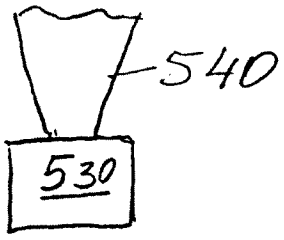
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530

FIG. 3

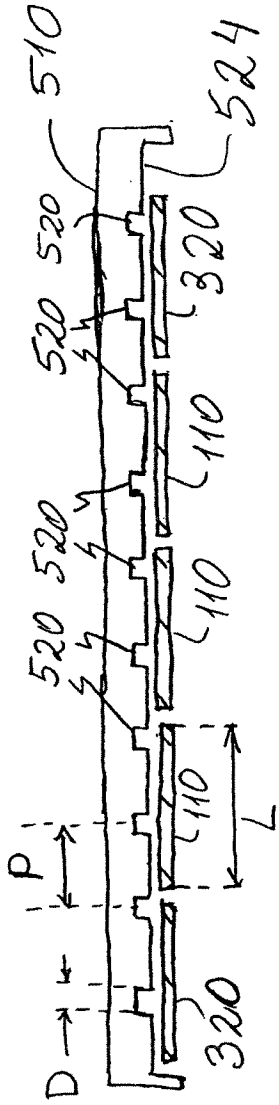


FIG. 4

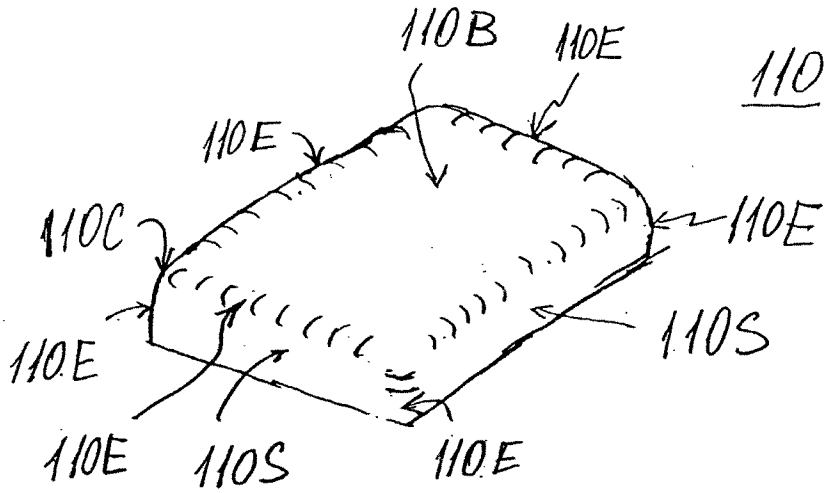


FIG. 5

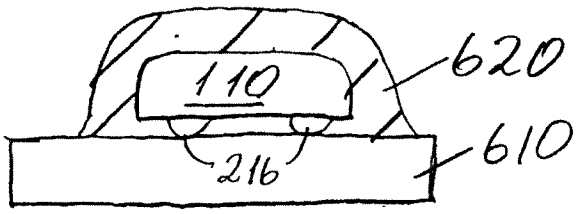
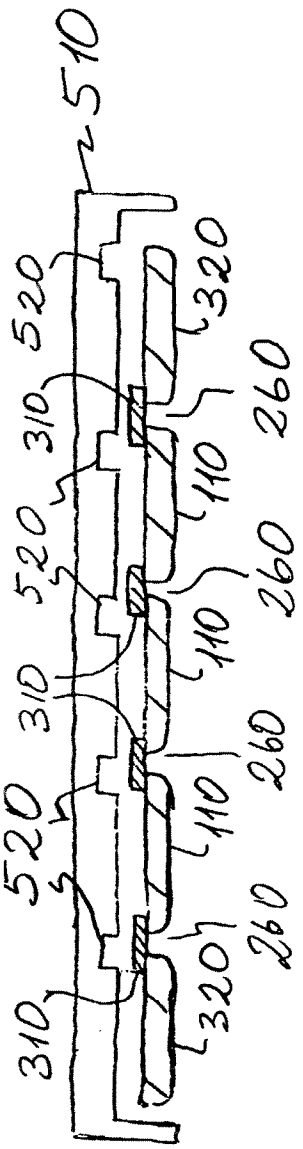


FIG. 6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320

FIG. 7

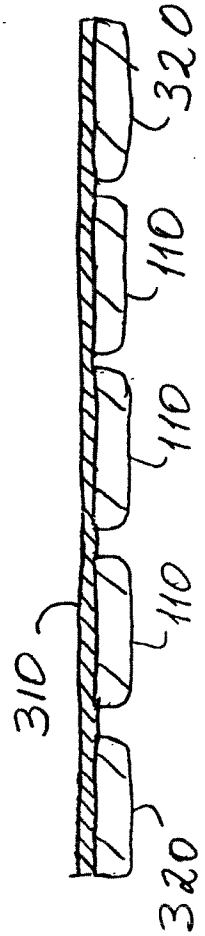
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FIG. 8

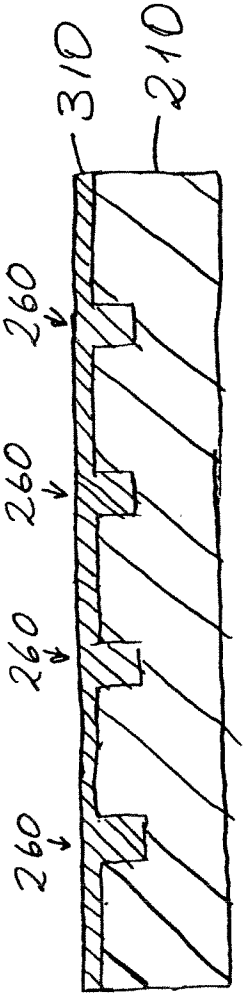

FIG. 9

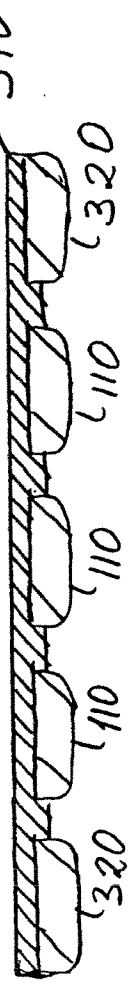

FIG. 10

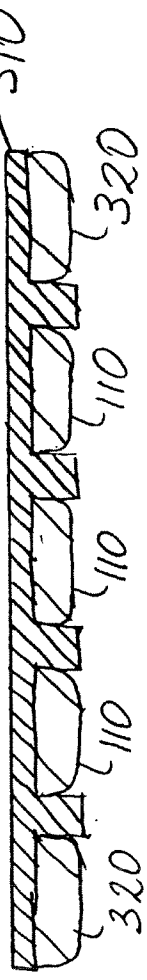

FIG. 11

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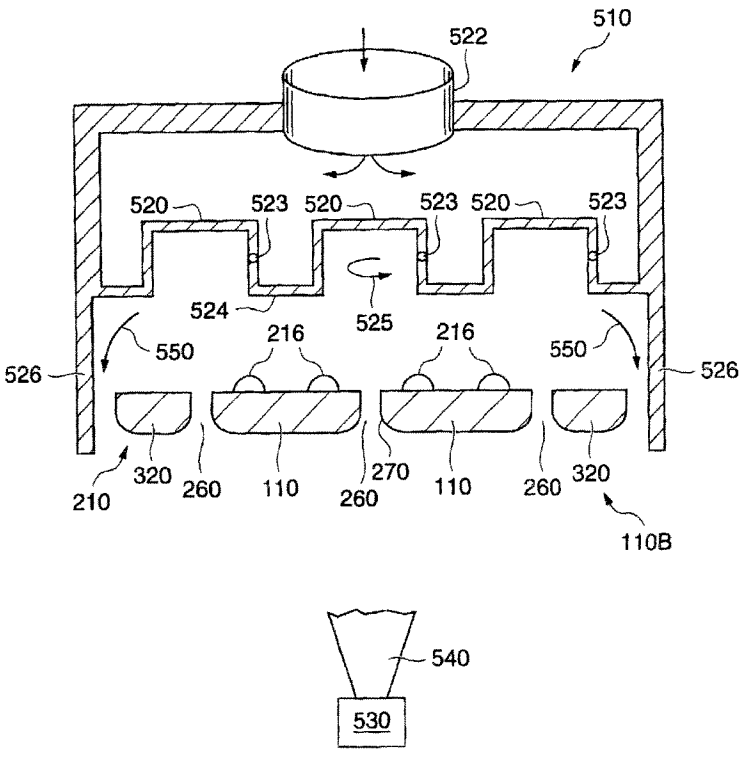
(54) Title: THINNING AND DICING OF SEMICONDUCTOR WAFERS USING DRY ETCH, AND OBTAINING SEMICONDUCTOR CHIPS WITH ROUNDED BOTTOM EDGES AND CORNERS



(57) Abstract: A semiconductor wafer (210) is diced before thinning. The wafer (210) is diced only part of the way through, to form grooves which are at least as deep as the final thickness of each chip to be obtained from the wafer. Then, the wafer is placed into a non-contact wafer holder (510), and the wafer backside is blanket etched with a dry etch, for example, atmospheric pressure plasma etch. The wafer is thinned until the grooves are exposed from the backside. The dry etch leaves the chip's backside smooth. After the grooves have been exposed, the dry etch is continued to remove damage from the chip sidewalls and to round the chip's bottom edges (110E) and corners (110C). As a result, the chip becomes more reliable, and in particular more resistant to thermal and other stresses.

WO 01/056063 A3

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THINNING AND DICING OF SEMICONDUCTOR WAFERS USING DRY ETCH, AND OBTAINING SEMICONDUCTOR CHIPS WITH ROUNDED BOTTOM EDGES AND CORNERS

BACKGROUND OF THE INVENTION

The present invention relates to thinning and dicing of semiconductor wafers using a dry etch.

In many semiconductor fabrication processes, when circuitry has been fabricated in a semiconductor wafer, the wafer is thinned and then diced into chips. The thinning is typically performed with mechanical lapping. Dicing is performed with a diamond saw or a laser. The diamond saw or the laser can be used to cut the wafer all the way through along scribe lines. Alternatively, the wafer is cut part of the way through, and then broken.

The thinning and dicing processes can damage the wafer. It is desirable to provide alternative processes that reduce wafer damage and prolong the lifetime of chips obtained from the wafer.

SUMMARY

Some embodiments of the present invention reduce or eliminate wafer damage and prolong the chip lifetime by dicing the wafer part of the way through and then thinning the wafer with a dry etch. The chip lifetime is prolonged because the dry etch removes damage from chip surfaces and rounds the chip's edges and corners.

More particularly, as illustrated in Fig. 1, a chip 110 obtained by prior art thinning and dicing techniques may have uneven, damaged surfaces 110B, 110S, with sharp bottom corners and edges. Surface 110B is the chip's backside, and surfaces 110S are sidewalls. The wafer has been thinned from backside 110B by mechanical lapping, and then diced along sidewalls 110S with a diamond saw or a laser apparatus. These thinning and dicing processes damage the backside 110B and sidewalls 110S. The damage may include chipped, jagged surfaces, and microcracks. When the chip 110 is later packaged and put into use, the chip is subjected to heating and cooling cycles. These cycles cause the chip's

packaging material (not shown) to exert stresses on the chip. Additional stresses can be developed inside the chip due to the thermal cycles, chip handling, or the presence of different materials or other non-uniformities inside the chip. Because the chip surfaces 110B, 110S are damaged, and because they intersect at sharp edges and corners, the stresses concentrate at isolated points on the chip surface. Further, microcracks weaken the chip's resistance to stress. As a result, the chip becomes less reliable. Cracks formed or extended by stresses in the chip can reach and damage the chip circuitry (not shown).

Dry etch provides smoother chip surfaces and rounded edges and corners. Damage is reduced or eliminated. The chip reliability is therefore improved.

In some embodiments of the present invention, the wafer is processed as follows. The wafer is diced to form grooves in the face side of the wafer. The grooves are at least as deep as the final thickness of each chip to be obtained from the wafer. Dicing can be performed with a diamond saw or a laser. The grooves' sidewalls can be damaged.

Then the wafer is placed into a non-contact wafer holder, and the wafer backside is etched with the dry etch until the grooves are exposed from the backside. The dry etch leaves the chips' backside smooth. In some embodiments, the dry etch continues after the grooves have been exposed from the backside. The etchant gets into the grooves and smoothens the chip sidewalls, removing at least some of the sidewall damage. The etchant also rounds the bottom corners and edges of the chips.

Suitable etches include atmospheric pressure plasma etches described, for example, in the PCT Application PCT/US97/18979 (WO 98/19337) filed October 27, 1997, incorporated herein by reference. These etches are fairly fast. Silicon can be etched at 10 μm/min.

In some embodiments, the dry etch is a blanket uniform etch of the wafer's flat backside surface. No masking layers are used on the backside surface.

The invention is not limited to the embodiments described above. In some embodiments, one or more openings are formed in a first surface of a semiconductor wafer along a boundary of one or more chips. The openings do not go through the wafer. The

wafer is placed into a non-contact wafer holder and thinned with a dry etch until the openings are exposed on a second side.

Other features of the invention are described below. The invention is defined by the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a side view of a prior art semiconductor chip.

Fig. 2A is a top view of a wafer being processed according to an embodiment of the present invention.

Fig. 2B shows a cross-section of the wafer of Fig. 2A along the lines II - II.

Figs. 3 and 4 are cross-sections illustration of a wafer and processing equipment during wafer thinning according to an embodiment of the present invention.

Fig. 5 is a perspective view of a chip processed according to an embodiment of the present invention.

Fig. 6 is a side view of a packaged chip processed according to an embodiment of the present invention.

Figs. 7 through 11 are cross-section illustrations of wafers being processed according to embodiments of the present invention.

DESCRIPTION OF SOME EMBODIMENTS

Fig. 2A is a top view of a semiconductor wafer 210 shown before the wafer is thinned with a dry etch. Fig. 2B is a cross sectional view of the wafer along the lines II-II in Fig. 2A. Circuitry has been fabricated in the wafer, and the wafer must now be divided into chips 110. The circuitry may include transistors, diodes, and other devices (not shown) manufactured in and over an active layer 220 (Fig. 2B) adjacent to the wafer top surface 210F (the surface shown in Fig. 2A). Optional conductive bumps 216 have been

manufactured on contact pads on top surface 210F of chips 110. The bumps will be used to connect the chips to wiring substrates (not shown), e.g., printed circuit boards.

The wafer thickness 240 has been sufficiently large to achieve suitable mechanical strength and heat dissipation during fabrication of the wafer circuitry. 720 μm is suitable for some silicon wafer fabrication processes. The wafer will now to be thinned to its final thickness 250. In some embodiments, the final thickness is 10-450 μm. These thickness figures are illustrative and not limiting.

After the circuitry and the bumps 216 were manufactured, grooves 260 were formed in the wafer top surface along scribe lines and, in particular, along the boundary of chips 110. The grooves could be formed by conventional dicing techniques, e.g. with a diamond saw or a laser. Other processes, e.g., a masked etch, could also be used. The grooves do not go through the wafer. The grooves are at least as deep as the final chip thickness 250. In some embodiments, the groove depth is 10-450 μm. The grooves will be exposed from the bottom during wafer thinning when the wafer back side 110B is etched, as described below.

The groove sidewall and bottom surfaces 270 can be damaged by dicing, as schematically shown by uneven lines in Figs. 2A, 2B.

Wafer 210 is placed in a non-contact wafer holder 510 (Fig. 3). Holder 510 includes one or more vortex chucks 520 having outlets in the holder's surface 524. Surface 524 faces the top surface of the wafer. Gas supplied under pressure through a conduit 522 enter chucks 520 through respective passages 523. Each passage is tangential to the chuck's cylindrical chamber when viewed from the top. A gas vortex 525 emitted by each chuck towards the wafer generates a low pressure zone near the chuck's vertical axis. In this zone, the wafer is drawn towards the chuck. At the same time, the gas vortices do not allow the wafer to touch the holder surface 524. Such wafer holders are described, for example, in U.S. patent application no. 09/456,135 "Non-Contact Workpiece Holder" filed by O. Siniaguine et al. on December 7, 1999 and incorporated herein by reference. Other suitable holders are described in PCT publication WO 99/46805 (TruSi Technologies, LLC, September 16, 1999) incorporated herein by reference. Other holders, for example, Bernoulli type holders, can also be used.

Wafer holder 510 is called "non-contact" because the top surface of the wafer does not contact the holder surface 524. However, the edge of the wafer can contact the holder's limitors 526 which extend around the wafer to restrict the wafer lateral motion. In some embodiments, holder 510 is mounted on a rotating carousel (not shown). The carousel rotation develops a centrifugal force that presses the wafer against one or more limitors 526. See PCT publication WO 99/26796 (TruSi Technologies, LLC, June 3, 1999).

The wafer backside surface 110B is etched with a dry etch. In Fig. 3, the etch is a blanket (unmasked) uniform etch of the wafer's flat semiconductor backside surface (e.g., silicon surface). The etch is atmospheric pressure plasma etch. Plasma generator 530 generates plasma 540 into which suitable reagents are injected. If the wafer is made of silicon, a CF4 etch can be used. See PCT publication WO 98/19337 (TruSi Technologies, LLC, May 7, 1998) incorporated herein by reference. A suitable etcher is type Tru-Etch 3000 (trademark) available from TruSi Technologies, LLC, of Sunnyvale, California. The dry etch thins the wafer until the grooves 260 are exposed from the bottom. When the grooves are exposed, the plasma enters the grooves and etches the groove sidewalls 270. The sidewalls become smoother as a result. The dicing damage becomes partially or completely removed from the sidewalls. The bottom corners and edges of chips 110 become rounded.

Advantageously, some atmospheric pressure plasma etching processes described in WO 98/19337 are fast. Silicon can be etched at the rate of about 10 μm/min. Other kinds of etches can also be used. The dry etch can be preceded by mechanical lapping of the wafer bottom surface 110B.

In some embodiments, before the backside etch, the groove depth 250 (Fig. 2) exceeds the final chip thickness by an amount needed to obtain the rounded edges and corners and smooth sidewalls for chips 110. The more the groove depth exceeds the final chip thickness, the longer the duration of the backside etch after the grooves have been exposed from the bottom. The bottom corners and edges become more rounded, and more time is allowed for sidewall damage removal. In some embodiments, the radius of the rounded corners is roughly 1.5 times the thickness of the material removed from the wafer backside after the grooves are exposed. The depth of the grooves also takes into account possible wafer non-uniformity, the non-uniformity of the dicing process that creates the

grooves, and the non-uniformity of the backside etch. If mechanical lapping or any other process is used to remove material from the wafer backside before the dry etch illustrated in Fig. 5, the non-uniformity of such process can also be taken into account. In some embodiments, the groove depth 250 exceeds the final chip thickness by 10 μm or more.

When the grooves 260 become exposed during the thinning etch of Fig. 3, chips 110 become separated from each other, but the chips are held in holder 510 by the vacuum forces developed by the gas vortices. The vortex chucks 520 are positioned close to each other to insure that each chip 110 will be adjacent to a low pressure zone developed by at least one chuck 520. In Fig. 4, "L" denotes the greatest lateral dimension of each chip 110. "P" is the distance between the centers of the adjacent chucks 520. "D" is the diameter of each chuck. "P" and "D" can vary for different chucks 520 in the same wafer holder. The diameter D of each vortex chuck should be small enough to prevent a chip from being sucked into the chuck. The chip should be balanced at a predetermined distance from the wafer holder surface 524 by the vacuum forces drawing the chip towards the holder and the opposite-direction forces generated between the chucks by the gas flowing away from the chucks. In some embodiments, $D < L/2$ and $P < L/2$ for all the chucks.

In some embodiments, each of P and D is less than one half of the shortest side of each rectangular chip 110.

In some embodiments, the distance between the adjacent chucks and the diameter of each chuck take into account the peripheral wafer portions 320 (Fig. 2A). Each of P and D is less than one half of the greatest lateral dimension, or of the longest or shortest side, of each portion 320.

Fig. 5 is a perspective view of a chip 110 after the etch. The chip is shown bottom side up. The chip's sidewalls 110S and bottom surface 110B are smooth. The edges 110E at which the sidewalls 110S meet with each other and with the bottom surface 110B are rounded, and so are the bottom corners 110C. The smooth surfaces and the rounded edges and corners prolong the chip's lifetime and improve the chip's reliability.

In Fig. 6, chip 110 has been mounted on a printed circuit board 610 using flip chip technology. Bumps 216 are soldered to the printed circuit board. Encapsulant 620 (suitable plastic) is deposited over the chip for protective purposes. The chip's smooth

surfaces and rounded edges and corners prolong the chip's lifetime. Similar advantages are achieved with non-flip-chip packaging.

In Fig. 7, the etch uniformity is improved by depositing a layer 310 over grooves 260 and wafer portions adjacent to the grooves. Layer 310 is deposited before the backside etch of the wafer. When chips 110 and peripheral portions 320 become separated during the backside etch, the layer 310 holds the chips and the portions 320 in the same position relative to each other. Therefore, the gaps between the chips 110 and the peripheral portions 320 remain uniform, and hence the chip sidewalls (the sidewalls of grooves 260) are etched uniformly. If some chips 110 were too close to each other or to peripheral portions 320, the chips' sidewalls could be etched too slowly, and less damage would be removed than desirable. Other sidewalls, farther from adjacent chips 110 or portions 320, could be undesirably overetched.

Layer 310 also relaxes the requirements for the distance between adjacent vortex chucks 520 and the diameter of each chuck since the chips 110 and peripheral portions 320 are held in position by layer 310 throughout the backside etch.

Layer 310 can be a sticky material which adheres to the wafer without additional adhesive. Alternatively, adhesives can be used. In some embodiments, layer 310 is polyimide. Polyimide is chosen because it does not react with etchants utilized in some thinning processes (e.g., CF4). The thickness of polyimide layer 310 is 1 μm to 200 μm in some embodiments. Other materials and thicknesses can also be used. In some embodiments, layer 310 is an adhesive tape such as described in US patent 5,888,883 issued on March 30, 1999 to Sasaki et al.

Layer 310 does not cover the middle portions of chips 110, including the bumps 216. The bumps, and any other uneven features of the chip top surface 210F, are believed to be capable of impeding adhesion of layer 310 to the wafer.

In some embodiments, layer 310 is pre-manufactured as a continuous sheet. Then openings are cut out in layer 310 at the location of the middle portions of chips 110. Then layer 310 is deposited.

Layer 310 can be deposited using known techniques. In some embodiments, layer 310 is deposited at atmospheric pressure using a roller to remove air bubbles. Alternatively, layer 310 can be laminated on the wafer in vacuum, with or without a roller.

In some embodiments, layer 310 covers peripheral portions 320. In Fig. 8, layer 310 covers the entire wafer. In some embodiments, the top surface of chips 110 is even, bumps 216 are absent.

The invention is not limited to layer 310 covering or exposing any particular features of the wafer.

Layer 310 prevents the plasma from going through the grooves 260 and damaging the circuitry at the top surface of the wafer. Gas emitted by chucks 520 flows down around the wafer as shown at 550 in Fig. 3, and impedes the plasma from flowing up around the wafer and reaching the wafer top surface. As indicated in the aforementioned U.S. patent application 09/456,135, the chuck density can be made high at the edge of wafer holder 510 to prevent the plasma from flowing up around the wafer. Gas can be made to flow down at all points around the wafer.

In Fig. 9, layer 310 has been deposited by a spin-on or spraying technique. Layer 310 fills grooves 260. (In contrast, in Figs. 7 and 8, the grooves are not filled.) Layer 310 in Fig. 9 can be polymer or some other material.

Fig. 10 shows the structure after the backside etch for Fig. 9. In the embodiment of Fig. 10, when layer 310 is exposed from the bottom, layer 310 is etched faster than the wafer substrate. Therefore, the bottom surface of layer 310 is higher than the bottom surface of chips 110 and peripheral portions 320. The bottom corners and edges of chips 110 have been exposed to the etchant, and have been rounded.

Fig. 11 illustrates an embodiment in which the layer 310 is etched slower than the wafer substrate. This is the case if layer 310 is polyimide, the wafer is a silicon wafer, and the etch is a CF4 plasma etch. Layer 310 is etched slowly, but the microloading effect causes the chips 110 to be etched faster at the bottom edges adjacent to layer 310. As a result, the bottom edges and corners of chips 110 are rounded.

After the etch of Fig. 10 or 11, layer 310 is removed. In some embodiments, polyimide layer 310 is removed by oxygen plasma.

The above embodiments illustrate but do not limit the invention. The invention is not limited to silicon wafers or any packaging technology. The invention is not limited to plasma etching, or to any particular etch chemistry or type of etcher. The invention is not limited to wafers containing multiple chips. In some embodiments, only one chip has been

fabricated in the wafer. The chip is extracted and the wafer peripheral portions 320 are discarded. The invention is not limited to unmasked or uniform backside etches. Other embodiments and variations are within the scope of the invention, as defined by the appended claims.

CLAIMS

1. A method for obtaining one or more chips from a semiconductor wafer, the method comprising:

forming one or more openings in a first surface of the semiconductor wafer along a boundary of the one or more chips, wherein the one or more openings do not go through the wafer; and

placing the wafer into a non-contact wafer holder and thinning the wafer with a dry etch to remove material from a second side of the wafer at least until the openings become exposed on the second side.

2. The method of Claim 1 wherein the one or more openings comprise a groove extending along the entire boundary of at least one chip.

3. The method of Claim 2 wherein the wafer holder comprises one or more vortex chucks each of which emits a gas vortex towards the wafer to hold the wafer in the holder.

4. The method of Claim 2 further comprising, after forming the one or more openings but before thinning the wafer, attaching the first side of the wafer to a layer which remains on the wafer while the wafer is thinned.

5. The method of Claim 2 further comprising, after forming the one or more openings, forming a protective layer on the first side over the openings, the protective layer protecting the first side of the wafer during the dry etch from an etchant penetrating through the openings from the second side and damaging the first side when the openings become exposed on the second side.

6. The method of Claim 5 wherein the layer does not cover the entire first side of the wafer.

7. The method of Claim 5 wherein the layer covers the entire first side of the wafer.

8. The method of Claim 2 wherein the dry etch comprises an atmospheric pressure plasma etch.

9. The method of Claim 2 wherein after the groove is exposed from the second surface, the dry etch continues and smoothens the groove's sidewall.

10. The method of Claim 2 wherein the semiconductor wafer comprises circuitry made at the first side of the wafer, the second side is a backside opposite to the first side, and the groove is formed along a scribe line on the first side.

11. The method of Claim 2 wherein the groove is formed with a diamond saw or a laser.

12. The method of Claim 2 wherein the dry etch rounds one or more of the edges and corners which are obtained on the second side of the wafer when the one or more openings are exposed.

13. The method of Claim 12 wherein the dry etch rounds all of the edges and corners on the second side of each semiconductor chip obtained from the wafer in the dry etch.

14. The method of Claim 2 wherein from a start of the thinning operation until the groove is exposed, the dry etch etches the second side of the wafer uniformly.

15. The method of Claim 2 wherein the entire dry etch is an unmasked etch of the second surface.

16. A semiconductor chip obtained by the method of Claim 1.

17. A semiconductor chip obtained by the method of Claim 2.

18. A semiconductor chip obtained by the method of Claim 12.

19. A semiconductor chip obtained by the method of Claim 13.

20. A semiconductor ship having a first surface that has a rounded edge or a rounded corner.

21. The semiconductor chip of Claim 20 in which all of the edges and corners of the first surface are rounded.

22. The semiconductor chip of Claim 20 wherein the first surface is a back surface of the chip, the chip having circuitry formed at its front surface which is opposite to the back surface.

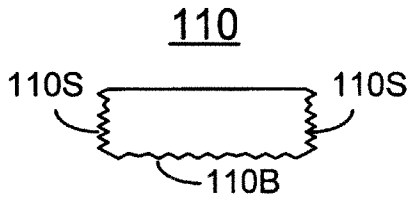
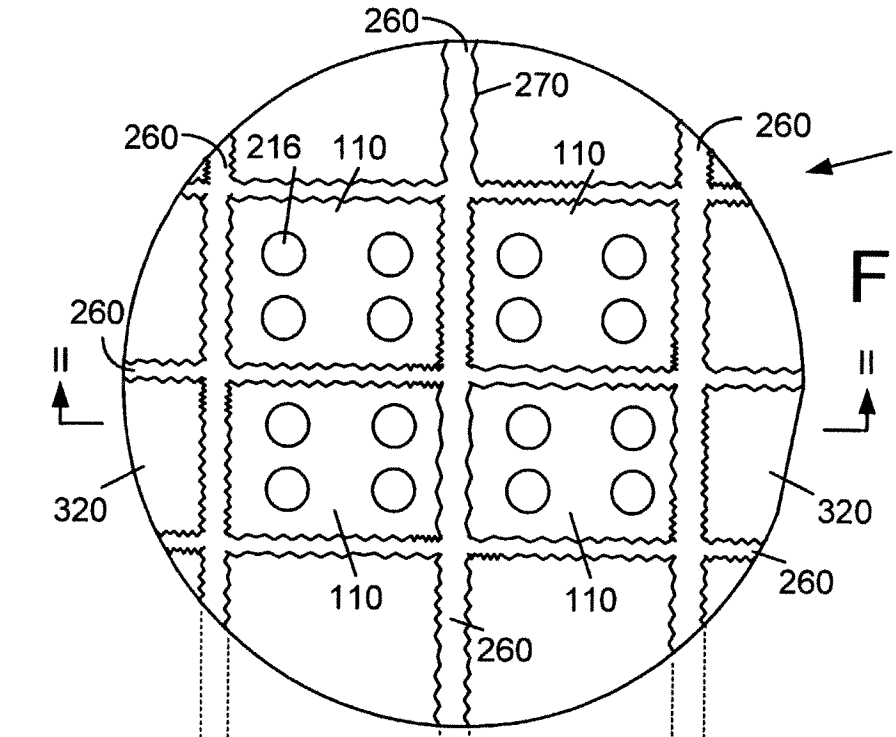


FIG. 1
(PRIOR ART)


260
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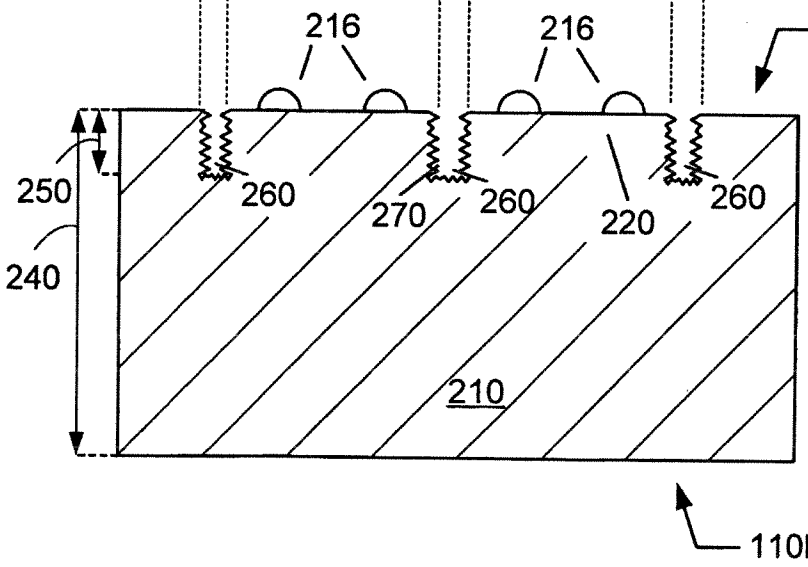
216
110
110
260
210
260
II
II
320
320
110
110
260
260

FIG. 2A


216
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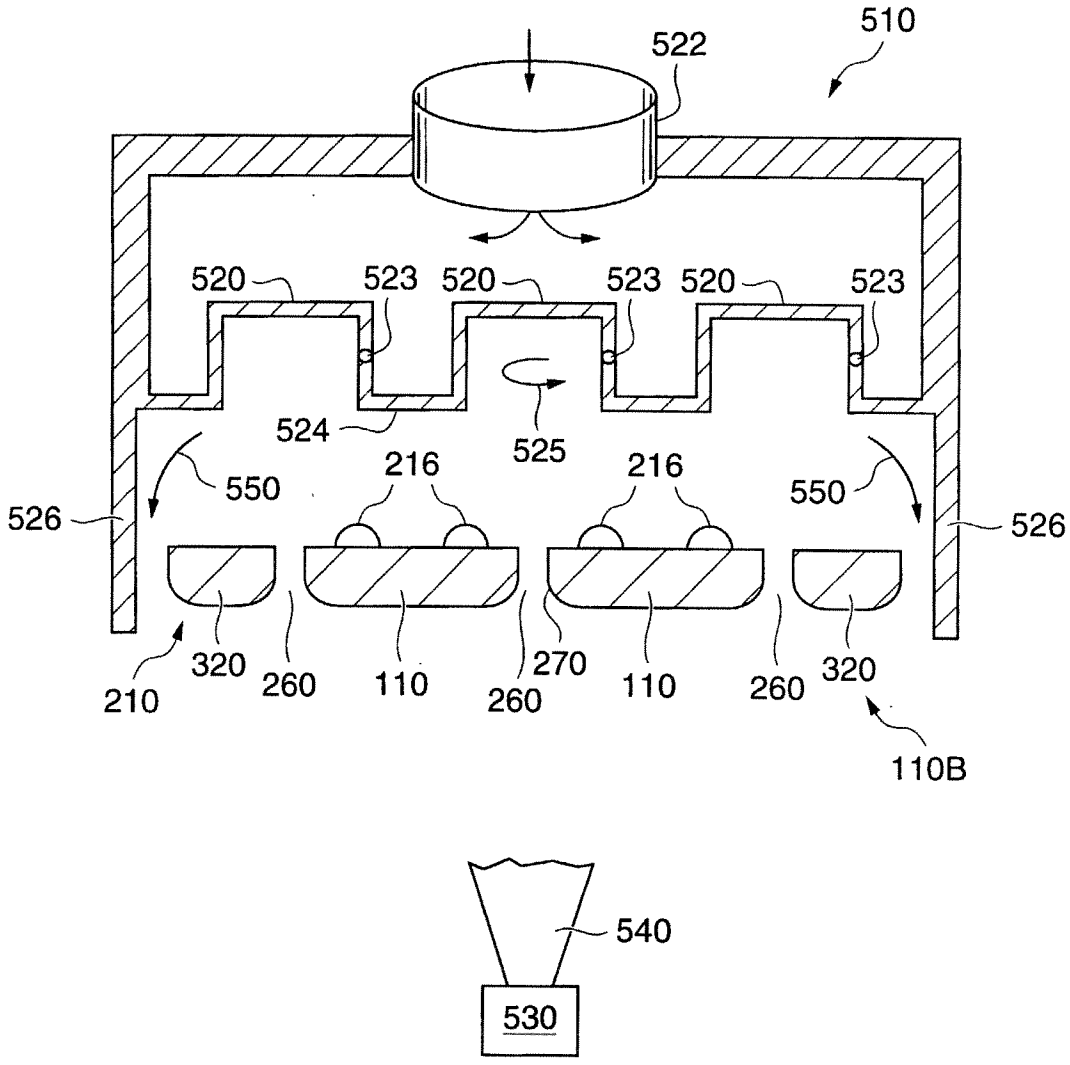
210F
250
240
260
270
260
220
260
210
110B

FIG. 2B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522
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110
260
320
110B
540
530

FIG. 3

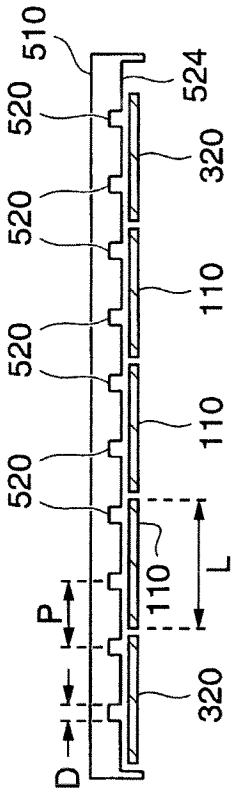


FIG. 4

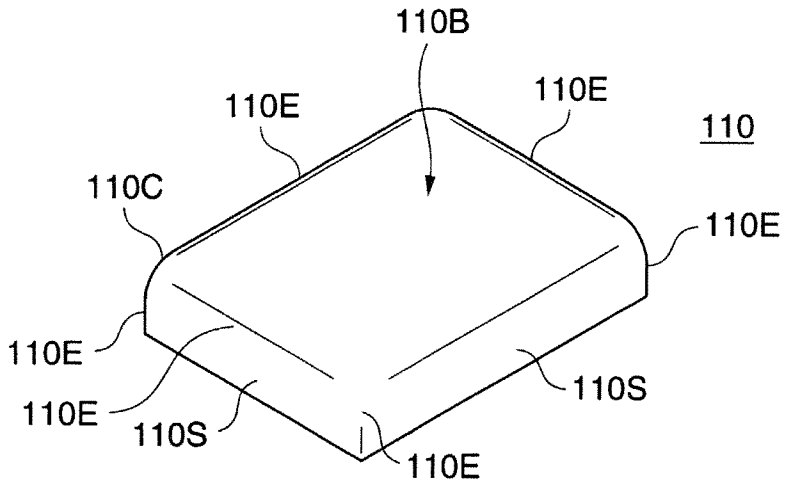


FIG. 5

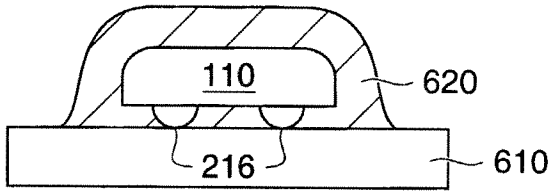
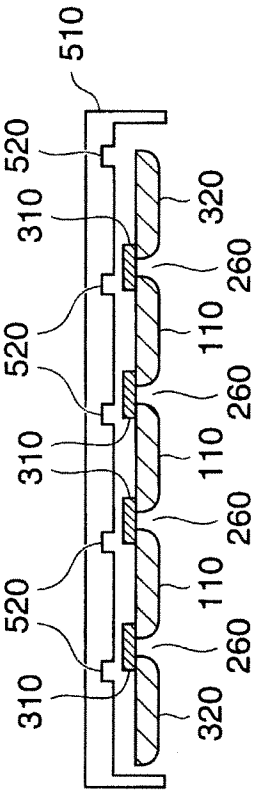


FIG. 6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520
310
320
260
110
520
260
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520
110
260
310
320

FIG. 7

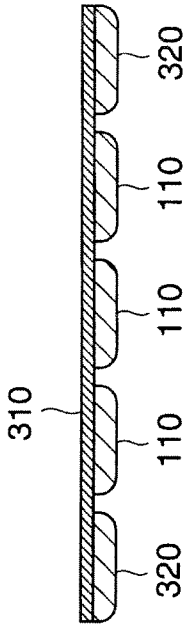
310
320
110
110
110
320

FIG. 8

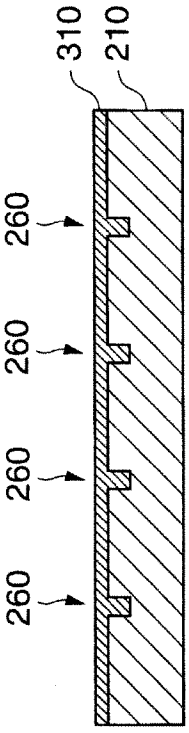

FIG. 9

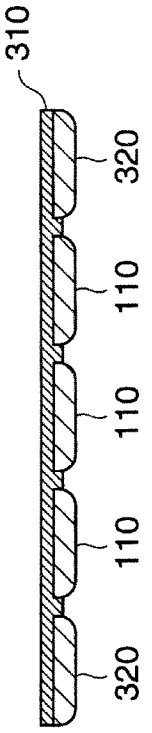

FIG. 10

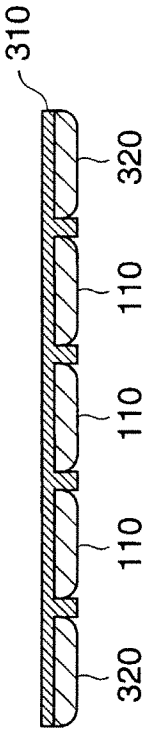

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/02544

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01L 21/301, 21/46, 21/44, 23/02
US CL : 438/113, 114, 460, 461, 462, 463, 464, 706; 257/678
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/113, 114, 460, 461, 462, 463, 464, 706; 257/678

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

JPO, EPO, Dew

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US 6,176,966 B1 (Tsujimoto et al) 23 January 2001 (23.01.01), Fig.1	1-21
A	US 6,004,867 A (Kim et al) 21 December 1999 (21.12.99), Col.5, line 16- Col.6, line 65.	1-21
A	US 3,991,296 (Kojima et al) 09 November 1976 (09.11.76), col.3, line 47 - Col.4, line49	1-21
X	US 3,739,463 (Aird et al) 19 June 1973 (19.06.73), Fig.9	20-22

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 30 APRIL 2001	Date of mailing of the international search report 12 JUN 2001
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DONGHEE KANG Telephone No. (703) 305-9147

Form PCT/ISA/210 (second sheet) (July 1998)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/02544

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See form PCT/ISA/206, Invitation To Pay Additional Fee's, mailed 24 March 2001. Applicant elected to pay all fee's.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.